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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 3558P027C

In re patent application of
Michael A. Vyvoda et al.

Serial No. 10/681,504

Group Art Unit: 2826

Filed: October 7, 2003

Examiner: Thomas L. Dickey

For: ELECTRICALLY ISOLATED PILLARS IN ACTIVE DEVICES

BRIEF ON APPEAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 18, 2005

To the Commissioner:

This Appeal Brief is being filed in triplicate along with authorization to charge deposit account 502302 for the appeal fee. Appellant hereby appeal the February 10, 2005 final rejection of claims 68-70 in the above-identified application to the Board of Patent Appeals and Interferences.

REAL PARTY IN INTEREST

The real party in interest is Matrix Semiconductor, Inc., a Delaware corporation.

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Pamela J. Squyres, reg. no. 52,246

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Vyvoda et al.

Application No.: 10/681,504

Filed: 10/07/2003

Title: Electrically Isolated Pillars in Active Devices

Attorney Docket No.: MA-075-a

Group Art Unit: 2826

Examiner: Thomas L. Dickey

Assistant Commissioner for Patents
PO Box 1450
Alexandria VA 22313-1450

July 18, 2005

FEE AUTHORIZATION

The Director is hereby authorized to charge deposit account 502302 for payment of the large-entity fee of $500.00 for filing a brief in support of an appeal under 37 CFR 41.20(b)(2). This authorization is provided in duplicate.

7/18/05
Date

Pamela J. Squyres, reg. no. 52,246

RELATED APPEALS AND INTERFERENCES

The undersigned is not aware of any related appeals and interferences.

STATUS OF CLAIMS

Claims 68-70 are pending in the Application. A listing of the appealed claims is presented in the APPENDIX.

Claims 68-70 have been finally rejected under 35 U.S.C. § 102(b) as being anticipated by Johnson et al., U.S. Patent No. 6,034,882 ("Johnson et al.").

STATUS OF AMENDMENTS

No amendments after final rejection were filed.

SUMMARY OF INVENTION

A monolithic three dimensional memory array is formed using a method to avoid formation of defects called *stringers*.

In conventional memories, memory cells are formed on a single level in the surface of a substrate, typically a monocrystalline silicon wafer. In contrast, a monolithic three dimensional memory array includes multiple memory levels formed *above* the substrate, stacked one atop another. Vertical stacking allows the memory to be highly dense.

In one form of monolithic three dimensional memory array, each memory level includes parallel bottom conductors, extending horizontally, and parallel top conductors, also extending horizontally, the top conductors above the bottom conductors. The top and bottom conductors are perpendicular to one another and parallel to the wafer surface, forming a cross-point array. Between each bottom conductor and each top conductor, at their intersection, is a pillar. Each memory cell includes a portion of a bottom conductor, a pillar, and a portion of a top conductor. The bottom conductor, pillar, and top conductor include doped silicon layers and a dielectric antifuse layer, arranged to form a P-N diode and an antifuse. The memory cell is a one-time programmable memory cell programmed by rupturing the antifuse.

A monolithic three dimensional memory array having such a structure and function is taught in Johnson et al., US Patent No. 6,034,882, owned by the assignee of the present invention.

The array of Johnson et al. was formed using a high degree of self-alignment. Briefly, 1) the layers of the bottom conductors and the pillars were blanket deposited, the pillar layers above the bottom conductor layers. The pillar layers were silicon layers. 2) A first pattern-and-etch step was performed to etch the deposited layers, forming first parallel rails, the first rails including the layers of the pillars and the layers of the bottom conductors. 3) After dielectric fill and planarization to expose the tops of the first rails, the layers of the top conductors were deposited. 4) A second pattern-and-etch step also formed parallel rails, these rails perpendicular to the first rails. This pattern-and-etch step etched the layers of the top conductors, then continued, etching the layers of the pillars. The second etch stopped before etching the bottom conductors.

As is well known, most etchants are selective, etching some materials but not others. Both pattern-and-etch steps etched only the active layers, the top conductor layers, the pillar layers, and the bottom conductor layers, but did not etch the intervening dielectric fill.

The layers of the bottom conductors were etched in only the first pattern-and-etch step, and thus were in the form of rails. The layers of the top conductors were etched in only the second pattern-and-etch step, and thus were also in the form of rails. The layers of the pillars, between the top conductor and bottom conductor layers, were etched in *both* pattern-and-etch steps, which were perpendicular to each other, and thus were in the form of pillars, each pillar having a square cross-section. Considering the cross-section of each pillar, two opposing edges of each pillar were aligned with the edges of the bottom conductor below it, while the other two opposing edges of the pillar were aligned with the edges of the top conductor above it.

This fabrication method minimized the number of masking steps, which are very expensive, and was thus advantageous. It suffered a disadvantage, however, which made the resulting memory prone to defects.

The etch during the two pattern-and-etch steps described was intended to be perfectly anisotropic, producing perfectly vertical sidewalls on the conductors and pillars. In reality, however, no etch is perfectly anisotropic, and some lateral etching of sidewalls occurs. The result is that rather than being perfectly vertical, etched sidewalls tend to be sloped so that an etched trench (the gap between rails, say) tends to be slightly wider at the top than at the bottom.

Thus the first pattern-and-etch step of Johnson et al. tended to produce parallel first rails which were slightly wider at the bottom than at the top. Next the gaps between the first rails were filled with dielectric material. The shape of each strip of dielectric material was the inverse of that of the rails, and necessarily wider at the top than at the bottom. Dielectric material, then, was slightly overhanging the material of the adjacent first rail.

After deposition of the top conductor layers, the second pattern-and-etch step was performed. This etch formed the top conductors, then continued to etch the pillar layers. Recall that the pillar layers are silicon, and that during the pillar etch, silicon is etched, while the dielectric fill is not. Thus between the pillars, overhanging dielectric material shielded a small volume of silicon from the etchant during the second pattern-and-etch step, preventing it from being removed as intended. These small remainders of silicon, called stringers, could connect a pillar to an adjacent pillar, forming a conductive path between structures that were intended to be electrically isolated, and creating a short.

Turning now to the present invention, the sequence of events is changed, creating a structure similar to that of Johnson et al., while avoiding this harmful stringer formation.

Fabrication in the present invention begins as in Johnson et al.: 1) The layers of the bottom conductors and of the pillars are deposited. 2) A first pattern-and-etch step is performed, forming parallel first rails.

At this point, however, is an important difference: 3) *Before* the dielectric fill is deposited between the first rails, in the present invention a second pattern-and-etch step is performed, perpendicular to the first, forming the pillars. No dielectric material intervenes between the pillars to shield any stringer material from etchant; thus no stringers are formed.

Fabrication continues: After dielectric fill and a planarization step to expose tops of the pillars, 5) the top conductor layers are deposited, and 6) a third pattern-and-etch step forms the top conductors.

Compared to Johnson et al., the method of the present invention requires an additional masking step, but stringer formation, to which Johnson et al. was susceptible, is avoided.

The present invention, then, is an array of memory cells having bottom conductors, pillars, and top conductors in which the pillars are substantially free of stringers.

ISSUES

The only issue is whether claim 68 is anticipated by Johnson et al. under 35 U.S.C. §103(b).

GROUPING OF CLAIMS

Claim 68-70 are the only claims at issue.

SUMMARY OF THE ARGUMENT

Claim 68 is patentable over Johnson et al. because, although stringers are not actually depicted in the idealized figures of Johnson et al., one skilled in the art at the time of the invention would reasonably expect stringers to be formed in the array of Johnson et al. at least some of the time.

ARGUMENT

Summarizing, claim 68 recites a monolithic 3-dimensional memory array comprising a first set of strips (bottom conductors), a second set of strips (top conductors) and a pillar between them; also included are third set of strips and a second pillar, the second pillar between the second strips and the third strips and belonging to a second memory level stacked above the first. The claim further specifies sloped sidewalls on the pillars and P- and N-doped silicon regions within the named components of the memory array. Claim 68 includes the limitation that each of the pillars is *substantially free of stringers.*

The Examiner has rejected claim 68 under 35 USC 102(b) as being anticipated by Johnson et al.

Recall that Claim 68 includes the limitation that "each of the pillars is substantially free of stringers." The disclosure of Johnson et al. is silent regarding the presence of stringers. The Examiner points out that the drawings of Johnson et al. do not show stringers, but it will be well understood by those skilled in the art that, for the sake of clarity, the representation in drawings is idealized, and it cannot be expected that every flaw and irregularity, including stringers, will be shown; thus the fact that stringers are not shown in the drawings cannot be construed as evidence of their absence.

The description in the specification of the present application, for example in paragraph [0008], shows how fabrication methods used by Johnson et al., for example starting at col. 13, line 26, and illustrated in Figs. 6(a) through 6(g), may tend to create stringers.

Specifically, an etch step actually likely to produce stringers, as described in the present application, is detailed in Johnson et al. at col. 14, lines 13 to 27, and the idealized resulting structure is shown in Fig. 6(g) of Johnson et al. For example, stringers may be formed connecting pillar 51a1 and pillar 51a2 in Fig. 6(g). In the present application, Fig. 3G illustrates an analogous structure formed using the same steps, but also shows the stringer S1 which may inadvertently be formed connecting analogous pillars 304P(1) and 304P(3).

As described, by using a different fabrication method, the memory of the present invention will not be susceptible to stringers.

In the final rejection of February 10, the Examiner declines to recognize the difference between Johnson et al. and the invention of claim 68, pointing out that "there are no stringers in figure 6(g) or anywhere in the disclosure of Johnson et al."

"Surely," the Examiner asks, "Applicant is not insisting that Johnson et al. have run through a list, from Aardvarks to Zulu Warriors, of all the things not found ... in their device?"

Appellants hasten to assure the Examiner that the failure of Johnson et al. to spell out the absence of aardvarks in their memory array is not considered license to assume aardvarks, bandicoots, cassowaries, or any other creature one skilled in the art would not reasonably expect to find there.

The standard to be applied when the presence or absence of a characteristic in a reference is not explicitly addressed in that reference is described in *Continental Can Co. USA v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991): "Such evidence must make clear that the missing descriptive matter is *necessarily present* in the thing described in the reference, and that it would be so recognized by persons of ordinary skill in the art." (Emphasis added.)

Claim 68 includes the limitation that "each of the pillars is substantially free of stringers." There is no description in Johnson et al. describing the *absence* of stringers. Thus in order for Johnson et al. to anticipate, it must be clear to one of ordinary skill in the art that the pillars of Johnson et al. *necessarily* have the characteristic recited in the claim, where that characteristic is the absence of stringers. The preferred method used to create the pillars in Johnson et al. is precisely that which in the present invention is shown to tend to create stringers; thus the *absence* of stringers required by the claim would *not* be assumed by one skilled in the art. That one or more pillars may conceivably be produced by the method of Johnson et al. that is free of stringers is irrelevant; the absence of stringers required by the claim must *necessarily* be present for Johnson et al. to anticipate claim 68. Since the *absence* of stringers is not *necessarily present*, the device of Johnson et al. does not anticipate the invention of claim 68.

A description of an invention in a patent specification cannot be expected to list all possible flaws; this is neither conventional nor required. Also, as is well understood, it is very common for a patent application to be filed before much, if any, experience with fabrication of the claimed device has been acquired, or defects recognized. Johnson et al. likely did not mention the danger of stringer formation in part because Johnson et al. did not anticipate this danger.

By the time of the present invention, however, more experience had been gained. While Appellants agree that one skilled in the art could not have expected the methods of Johnson et al. to produce a monolithic three dimensional memory array infested with Zulu warriors, Appellants maintain that such skilled artisan, would, in fact, have had a reasonable expectation of finding stringers in such a memory at least some of the time. One skilled in the art at the time of the invention would not have expected the memory of Johnson et al. to be substantially free of stringers, as recited in claim 68. Thus Appellants respectfully assert that Johnson et al. does not anticipate claim 68 or its dependent claims 69 and 70.

CONCLUSION

Accordingly, Appellant respectfully solicits the Honorable Board of Patent Appeals and Interferences to reverse the rejections of the pending claims and pass this application on to allowance.

Respectfully submitted,

Jul 18, 2005
Date

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This Appeal Brief is being filed in triplicate together with authorization to charge $500 (large entity) covering the appeal fee to the undersigned deposit account 502302. If this fee is deemed to be insufficient, authorization is hereby given to charge any deficiency (or credit any balance) to the undersigned deposit account 502302.

APPENDIX

68. A monolithic 3-dimensional memory array comprising:

a first set of strips including a first terminal;

a second set of strips including a second terminal;

a third set of strips including a third terminal;

a first pillar having at least one side wall with a slightly positive slope, said pillar disposed between and connecting said first and second sets of strips, and including a first P doped silicon region, a first N doped silicon region and a first insulating region;

a second pillar having at least one side wall with a slightly positive slope, said pillar disposed between and connecting said second and third sets of strips, and including a second P doped silicon region, a second N doped silicon region and a second insulating region;

wherein each of the pillars is substantially free of stringers.

69. The memory of Claim 68, wherein each of said first and second insulating regions is disposed between the respective P and N doped silicon regions.

70. The memory of Claim 68, wherein the respective P and N doped silicon regions abut one another.